IN THE SPECIFICATION:

At page 1, after the title, please insert:

RELATED APPLICATION DATA

This patent application is a continuation-in-part of co-pending U.S. Patent Application Serial Number 09/063,335, filed on April 20, 1998, entitled "Method and Apparatus for Providing a Virtual Desktop System Architecture," now having an abandoned status.

Please amend the two paragraphs beginning at page 11, line 9, as follows:

One or more embodiments of the invention may implement the load distribution mechanisms described in U. S. Patent Application Serial No. 09/513,655, filed on February 25, 2000, entitled "Method and Apparatus for Distributing Load in a Computer Environment", and assigned to the present assignee, the specification of which is herein incorporated by reference.

One or more embodiments of the invention may also implement the mechanisms for improved resource utilization described in U. S. Patent Application Serial No. 09/513,652, filed on February 25, 2000, entitled "Method and Apparatus for Improving Utilization of a Resource on a Shared Client", and assigned to the present assignee, the specification of which is incorporated herein by reference.

Please replace the paragraph beginning at page 16, line 10, with the following rewritten paragraph:

In one embodiment of the invention, the CPU 213 is a microprocessor manufactured by Motorola, such as the 680X0 processor or a microprocessor manufactured by Intel, such as the 80X86, or PENTIUM ~~Pentium~~ processor, or a SPARC microprocessor from Sun Microsystems. However, any other suitable microprocessor or microcomputer may be utilized. Main memory 215 is comprised of dynamic random access memory (DRAM). Video memory 214 is a dual-ported video random access memory. One port of the video memory 214 is coupled to video amplifier 216. The video amplifier 216 is used to drive the cathode ray tube (CRT) raster monitor 217. Video amplifier 216 is well known in the art and may be implemented by any suitable apparatus. This circuitry converts pixel data stored in video memory 214 to a raster signal suitable for use by monitor 217. Monitor 217 is a type of monitor suitable for displaying graphic images.

Please replace the paragraph beginning at page 21, line 1, with the following rewritten paragraph:

An embedded processor 304 may be, for example, a SPARC-2ep ~~Sparc2ep~~ with coupled flash memory 305 and DRAM 306. The USB controller 301, network controller 302 and embedded processor 304 are all coupled to the PCI bus 319. Also coupled to the PCI bus 319 is the video controller 309 with associated SGRAM 307. The video controller 309 may be for example, an ATI RagePro+ frame buffer controller that provides SVGA output on line 315. Data is optionally provided in and out of the video controller through video decoder 310 and video encoder 311 respectively. This data may comprise digital or analog video signals (e. g., NTSC (National Television Systems Committee), PAL (Phase Alternate Line), etc.). A smart card interface 308 may also be coupled to the video controller 309.